The idea behind the tee topology is to achieve a higher voltage drop across the resistor network by drawing current from an additional source other than the signal input. In this case, that source is ground via $R3$. As with the standard inverting circuit, input current, i_{IN}, flows through $R1$ and $R2$ and creates v_{TEE} in the same way that v_O would be created in the standard circuit.

$$v_{TEE} = v_- - i_{IN}R2 = 0 - \frac{v_{IN}}{R1}R2 = -v_{IN}\frac{R2}{R1}$$

This works, because i_{IN} has nowhere to go but through R2, assuming an approximately ideal op-amp. Because v_{TEE} has already been established, there is a voltage drop across $R3$ with an accompanying current. The input current and i_{R3} combine to form the total current that flows through R4 to develop the final output voltage,

$$v_O = v_{TEE} - (i_{IN} + i_{R3})R4 = v_{TEE} - \left[i_{IN} + \frac{0 - v_{TEE}}{R3}\right]R4 = -v_{IN}\frac{R2}{R1} - \left[\frac{v_{IN}}{R1} + v_{IN}\frac{R2}{R1R3}\right]R4$$

$$= -v_{IN}\left[\frac{R2}{R1} + \frac{R4}{R1} + \frac{R2R4}{R1R3}\right] = -\frac{v_{IN}}{R1}\left[R2 + R4\left(1 + \frac{R2}{R3}\right)\right]$$

A combination of high circuit gain and high input resistance is now achievable using resistors not exceeding a practical limit of 1 MΩ. The circuit in Fig. 14.21 produces a gain of approximately –1,000 with an input resistance of 1 MΩ.

14.5 SUMMATION AMPLIFIER CIRCUITS

It is becoming clear that op-amps are very flexible analog building blocks. Aside from basic amplification, op-amp circuits can be designed to perform mathematical operations. Decades ago, analog computers were built around op-amps constructed from vacuum tubes rather than integrated circuits. These computers were capable of advanced functions including multiplication, division, exponents, and logarithms. Analog computers operate on voltage levels rather than bits and bytes.

Although the typical digital system may not benefit much from complex analog computation circuits, basic op-amp summation circuit analysis may prove useful in designing for various combinations of input signals and bias voltages. Figure 14.22 shows a basic summation circuit built on the

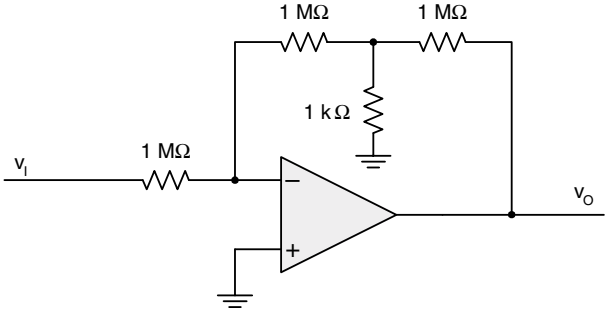

FIGURE 14.21 High gain/high input resistance inverting circuit.

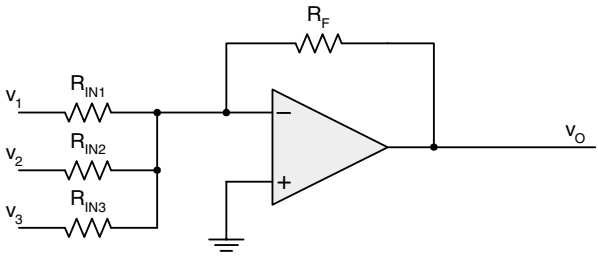

FIGURE 14.22 Summation circuit.

inverting topology. Each input is unaffected by the others, because the negative terminal is always at 0 V by reason of the virtual short. Therefore, each input resistor contributes an input current component determined by Ohm's law. These currents add and collectively pass through the feedback resistor to create an output voltage.

A weighted summation can be designed by individually selecting input resistors according to the application requirements. If the input resistors are all equal, the gain ratios for each input signal are equal, and the summation is balanced.

$$v_O = -\frac{R_F}{R_{IN}}[v_1 + v_2 + v_3]$$

Similarly, a noninverting circuit can be used to combine multiple input voltages without the –1 factor as shown in Fig. 14.23. Although usually referred to as a *noninverting summer,* this is more of an averaging circuit than a summer. The input voltages are averaged by the input resistor network, and this average level is then multiplied by the gain of the noninverting circuit.

Analyzing the input resistor network can be difficult without a common circuit-analysis trick that relies on the principle of *superposition*. Superposition works with a linear transfer function that relates an output to multiple inputs multiplied by some gain factor. For example, two signals, V_1 and V_2, add together and are multiplied to yield an output voltage: $V_O = A(V_1 + V_2)$. By the principle of superposition, the input terms can be broken up, computed separately, and then recombined at the output to yield a final expression: $V_{O1} = AV_1$ and $V_{O2} = AV_2$, thus $V_O = V_{O1} + V_{O2} = A(V_1 + V_2)$. Superposition works only when the transfer function is linear.

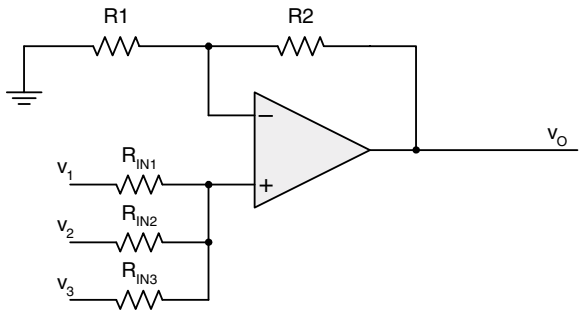

FIGURE 14.23 Noninverting summation circuit.